NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
B.Tech. in Electronics & Communication Engineering
Semester – V
Department Elective I

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Course Code	**2ECDE54**
Course Title	**System on Chip Design**

Course Outcomes (COs):
At the end of the course, the students will be able to

1. Design, optimize, and program a modern System-on-a-Chip.
2. Analyse a computational task; characterize its computational requirements for SoC.
3. Identify performance bottlenecks and explore a rich design space of solution.
4. Implement hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software co-design.

Syllabus: **Teaching hours: 45**

UNIT I: Introduction to System Approach **05**
Motivation, design, programming, optimization, and use of modern System-on-a-Chip (SoC) architectures, Components in the system: processor, memory and connectivity. Hardware and Software in the SoC, programmability versus performance. Approaches to designing a SoC.

UNIT II: Basics SoC Chip **06**
Time, Area, Power, Reliability, and Configurability: Design-space formulation and exploration, Costs and metrics (energy, area, runtime, reliability and predictability), Quantitative design and analysis.

UNIT III: Processors **06**
Choosing processors for the SoC, Basic concepts in processor architectures, Examples of processors for SoC: Vectors, VLIW processors and superscalar processors, Soft Processors, Custom Designed Accelerators.

UNIT IV: Memory Design **06**
System-on-Chip and Board-Based Systems, SoC External Memory DDR, Flash, SoC Internal Memory: Placement, Size of Memory, Scratchpads and Cache Memory, SoC (On-Die) Memory Systems, Board-based (Off-Die) Memory System, Interaction between processor and memory.

UNIT V: Interconnect Architectures **07**
Bus: Basic Architecture, SoC Standard Buses (AMBA, Core Connect) Network on Chip (NoC) Architecture, NoC with Switch Interconnects, Layered Architecture and Network Interface Unit.

UNIT VI: Customization and Configurability **05**
SoC Customization, Processor Customization Approaches, Customizing Instruction Processors Reconfigurable Technologies, Reconfiguration Overhead Analysis, Trade-Off Analysis: Reconfigurable Parallelism, Mapping the design into reconfigurable logic, High-Level Synthesis (HLS): Coding C to Gates, Coding HLS Accelerators.

UNIT VII: SoC Design Methodologies and Tools **07**
HW/SW co-design: analysis, partitioning, real-time scheduling, hardware acceleration, Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems, Transaction-Level Modeling (TLM), Electronic System-Level (ESL) languages: SystemC; High-Level Synthesis (HLS): allocation, scheduling, binding, resource sharing, pipelining, SoC and IP integration, verification and test.

UNIT VIII: Applications of SoCs **03**

Practical applications of systems on the chip. Applications in cryptography. Applications of the SoC for image processing, video and 3D graphics. Other applications, Next Generation challenges of SoC Design, Case studies.

Self-Study:

The self-study content will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:

Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings:

1. W. Wolf, Modern VLSI Design: IP Based Design, Person Education
2. M. J. Flynn, W. Luk, Computer System Design: System-on-Chip, John Wiley & Sons
3. S. Sutherland, RTL Modelling with System Verilog for Simulation and Synthesis, Create Space Independent Publishing
4. D. Thomas, Logic Design and Verification Using System Verilog, Create Space Independent Publishing
5. S. Pasricha, N Dutt, On-Chip Communication Architectures: System-on-Chip Interconnect, Morgan Kaufmann

L= Lecture, T= Tutorial, P= Practical, C= Credit