NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M. Tech. in Electronics and Communication Engineering (Embedded System)
M.Tech. Semester - II
Department Elective III

L	T	P	C
2	-	2	3

Course Code	**3EC32D305**
Course Title	**High Performance Computing**

Course Outcomes (COs):

At the end of the course, students will be able to -

1. Comprehend parallel processing mechanism and analyze the issues related with the High Performance Computing.
2. Program graphics processor using CUDA.
3. Propose Power aware computing and communication for high performance computing.

Syllabus: **Teaching Hours:**

UNIT I: Parallel Processing Concepts **10**

Levels of parallelism - instruction, transaction, task, thread, memory, and function, Models - SIMD, MIMD, SIMT, SPMD, and Dataflow Models, Demand-driven Computation, Architectures - N-wide superscalar architectures, multi-core, multi-threaded, Memory hierarchy and transaction specific memory design , Thread Organization

UNIT II: Graphics Processor Architecture **08**

GPU Architecture, Parallel Programming with CUDA: Processor Architecture, Interconnect, Communication, Memory Organization, and Programming Models in high performance computing architectures

UNIT III: Fundamental Design Issues in Parallel Computing **07**

Synchronization, Scheduling, Job Allocation, Job Partitioning, Dependency Analysis, Mapping Parallel Algorithms onto Parallel Architectures, and Performance Analysis of Parallel Algorithms

UNIT IV:Power-Aware Computing and Communication **05**

Power-aware Processing Techniques, Power-aware Memory Design, Power-aware Interconnect Design, Software Power Management, Recent Trends in High Performance Computing

Self-Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:

Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. Kai Hwang, Naresh Jotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability, Tata McGraw Hill
2. David Kirk, Wen-mei Hwu Programming Massively Parallel Processors: A Hands-on Approach, Morgan Kaufmann
3. John Cheng, Max Grossman, and Ty McKercher Professional CUDA C Programming, John Wiley
4. David Culler, Jaswinder Pal Singh, Parallel Computer Architecture: A hardware/Software Approach, Morgan Kaufmann.
5. David A. Bader (Ed.), Chapman and Hall, Petascale Computing: Algorithms and Applications, CRC Computational Science Series.

L = Lecture, T = Tutorial, P = Practical, C = Credit