NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M.Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech. Semester - II
Department Elective III

L	T	P	C
2	-	2	3

Course Code	**3EC12D302**
Course Title	**Memory Technology**

Course Outcomes (COs):

At the end of the course, students will be able to -

1. Comprehend architecture of RAM and non-volatile memory.
2. Apply reliability modelling and failure modes to memory design.
3. Design the memory cell using advanced technology.

Syllabus: **Teaching Hours:**

UNIT I: Static Random Access Memory Technologies **05**

MOS RAM technologies, SRAMs, architecture, SRAM cell and peripheral, Circuit operation, SRAM Technologies, SOI Technology, advanced SRAM architectures and technologies, DRAM technology development, CMOS DRAMs cell, theory and advanced cell structures

UNIT II: Embedded Memory Designs **08**

Nonvolatile memories, MOS ROMs, PROMs, EPROMs, One-Time Programmable EPROMS, EEPROM technology and architecture, Nonvolatile SRAM-Flash Memories, advanced Flash Memory architecture

UNIT III: Failure Memory Directions **09**

Memory failure modes, reliability modelling, Prediction design for reliability, reliability test structures, reliability screening and qualification, radiation effects, radiation hardening, process and techniques, Radiation hardened memory characteristics, soft errors

UNIT IV: Advanced Memory Designs **08**

Ferroelectric random access memories (FRAMs), Gallium arsenide FRAMs, Analog memories, Magneto resistive RAMs, Experimental memory devices, Memory hybrids and MCMs (2D), Memory stacks and MCMs(3D), memory cards, high density memory packaging

Self-Study:

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:

Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. Ashok K. Sharma, Advanced Semiconductor Memories: Architectures, Designs, and Applications, John Wiley
2. Ashok K. Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE Press
3. Kiyoo Itoh, VLSI Memory Chip Design, Springer International Edition
4. Santosh K. Kurinec, Krzysztof Iniewski, Nanoscale Semiconductor Memories: Technology and Applications, CRC Press

L = Lecture, T = Tutorial, P = Practical, C = Credit