0.25V Bulk Driven Variable Gain Amplifier using $g_{mb}/I_{drain}$ Method for Ultra-Low Power Low Voltage Biomedical Applications

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Abstract—The ultra-low power and low voltage is a significant requirement for the portable biomedical instrument. This paper proposed the bulk driven variable gain amplifier for the analog front end of digital hearing aid. The class AB operational Transconductance(OTA) Amplifier with bulk driven inputs is used with a non-tailed differential amplifier. Also, graphical method $g_{mb}/I_{drain}$ is used for designing aspect ratio of MOS transistor which is simplest compared to the analytical method. The total power dissipation is 6.5nW for a gain level at a gain of 31dB. The simulation is performed using SPICE in 0.18µm CMOS technology with supply voltage 0.25V.

Keywords—Ultra-Low Power, Bulk Driven MOS, Variable Gain Amplifier, Automatic Gain Control Circuits, Analog Front End.

I. INTRODUCTION

Nowadays, portable Biomedical electronic systems require complex integrated circuits with higher performance which can effectively work with ultra-low power supply [1]. The Biomedical Device like Digital Hearing Aid performs multifunction like Wireless Bluetooth Streaming, Smartphone Connectivity, and Smaller, Sleeker Designs. This higher performance required a large amount of power dissipation from a small size zinc-air battery. Figure 1 shows a block diagram of Digital Hearing Aid where analog front end consumes 61.8% of power from the total budget [2] – [10]. So it’s necessary to achieve low power dissipation, high-performance, and programmability to expand battery life and to offer a convenient hearing to the users.

The analog front end of digital hearing aid is used with gain compression principal where for input level gain is high and for high input signal level, the gain is kept at a constant level. The Automatic Gain control is most commonly used to perform this task in which a variable gain amplifier is utilized. The possible circuit arrangement used in the analog front end as shown in Figure 2.

The paper [2] utilize Gain Variations: -1dB to 50dB 0.5dB Step with high Gain from Feedback resistor and low gain compression principal where for input level gain is high and for high input signal level, the gain is kept at a constant level. The Automatic Gain control is most commonly used to perform this task in which a variable gain amplifier is utilized. The possible circuit arrangement used in the analog front end as shown in Figure 2.

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The paper is organized as follows: Section I with Introduction and literature survey, Section II with Design methodology for OTA and Section III with Variable Gain Amplifier followed by conclusion and references.

II. DESIGN METHODOLOGY

A. Class AB Topology and Description

The Two-Stage Class AB OTA is selected for the preamplifier of digital hearing aid. The first stage is a non-tailed differential amplifier followed by a Miller compensated second stage. The gain of the preamplifier is changed by changing the output resistance of the second stage which behaves as a variable gain amplifier.

Figure 3 Block Diagram of OTA

Figure 4 shows the circuit diagram of OTA [13] with first stage transistor(Q2-Q9) and second stage with (Q10- Q11) biasing circuits(Q1), compensating capacitor Cc, and load capacitor CL. The Transistors Q2 and Q5 formed a differential pair, with their gates biased by a diode-connected transistor (Q3, Q4) and a current sink (Q6, Q7). The bulk terminals of Q2 and Q5 are cross-connected with the bulk terminals of Q3 and Q4, respectively. The differential input signal is applied between the bulk terminals of Q2, Q4 on one side and the bulk terminals of Q3, Q5 on the other, hence change in their threshold voltages. The gates and bulk of Q2-Q3 and Q4-Q5 shorted for simultaneous controlled, hence drain currents of Q2 and Q5 are modified result in boosting the resulting transconductance to a higher value. The special features of circuits are:

I. Non-Tailed Configuration & Symmetrical Structure
II. Insensitive to input common-mode variations & High Output voltage swing
III. The First Stage is truly differential amplifier with cross-coupled Bulk Driven pairs

The second gain stage of the OTA is formed by the transistor Q10, loaded by the transistor Q11 with compensating capacitor as feedback to keep both poles far away to improve stability and phase margin. The second stage gain is higher than the first stage and also zero z1 introduced because of Cc, compensated by design consideration of zero z1 placed ten times far away from GBW.

B. Circuit Design Methodology

The two-stage OTA is designed with the following specifications as listed in Table. I by considering biomedical applications.

The small-signal analysis gives the following important relation.
I. Effective Transconductance of Input Stage:
\[ g_{meff} = 2g_{m1} \]

II. DC Value of the Gain:
\[ A_{dc} = \frac{-2g_{m1}}{g_{m2}} \]

III. Gain Bandwidth Product(GBW):
\[ GBW = \frac{2g_{m1}}{C_c} \]

The Aspect Ratio of all MOS transistors is calculated using gmb/Idrain(NMOS/PMOS) Method which is originally proposed for Gate Driven Transistor [14]. In this paper, the gmb/Idrain method is used for bulk driven pairs also. The DC characteristics of both NMOS and PMOS are plotted and gmb/Idrain (for PMOS) and gml/Idrain (for NMOS) curve is simulated with reference to Idrain/(W/L), (as shown in Figure 5). Initially, \( I_{d} = \frac{g_{m} V_{ds}}{2} \) followed by \( V_{gs} \) for \( I_{d} = \frac{g_{m} V_{ds}}{2} \) curve is plotted, then gmb/Idrain for PMOS and gml/Idrain for NMOS curve is simulated with reference to Idrain/(W/L). The transconductance of all-transistor is calculated based on the subthreshold operation. The design steps are as follows.

Step 1: Calculation of Total Bias Current:
Considering only the thermal noise of the bulk driven input differential pair with the noise bandwidth is (\( \pi /2 \)) GBW and \( \text{Vinmax} = \frac{VDD}{2} \), the biasing current \( I_{b} \) for different inversions region can be calculated as follows:
\[ I_{total} = DR^2 \sqrt{\frac{I_{gb}}{2n_p V_{T} k T}} \]
where, \( n_p = 1.35 \), \( n = 0.31 \). \( V_T = \text{Thermal Voltage} \). For better noise performance, \( I_{D1} = I_{D2} = I_{total}/4 = I_{bias} \) and Q1 = Q6 = Q7.

Step 2: Calculation of (W/L)_1,6,7:

The gm is in the subthreshold region is given by:
\[ g_{ml} = \frac{m\overline{I}}{m_{t1}} \]

where the subthreshold slope parameter \( m \) is a technology-dependent constant (usually 1<\( m < 2 \)). For \( I_{bias} = 3nA \), the corresponding \( g_{ml}/Idrain \) Vs Idrain/(W/L) graph is plotted (Figure 5) and the aspect ratio
\[ \frac{W}{L}_{1,6,7} = 29.12 \]

Step 3: Calculation of (W/L)_9:

The value of \( I_{gb} = I_{D9} \) almost equal to \( I_{bias} \), hence from Figure 5,
\[ \frac{W}{L}_{9} = 29.7 \]

Step 4: Calculation of (W/L)_10:

The second stage gain is high compared to the first stage by keeping \( I_{D10} = 10I_{D9} = 30nA \).
Step 5: Calculating \( \frac{W}{L} \):

The PMOS transistors are bulk driven input pairs of the non-tailed differential amplifier. For the selected configuration, the transconductance of bulk driven MOS transistor \( g_{mb1} \) approximately equal to 0.2-0.5 smaller than \( g_{m1} \). The \( g_{m1} \) is calculated based on the subthreshold operation. The PMOS drain characteristics curve is plotted for \( g_{mb}/I_{drain} \) Vs \( I_{drain}/(W/L) \). From Figure 6, the aspect ratio is:

\[
\left( \frac{W}{L} \right) = 14.6 \quad (9)
\]

Step 6: Calculating \( W/L \):

In this step, the current sink transitory \( Q_{11} \) is designed using \( g_{m}/I_{drain} \) method because it is not bulk driven. The \( I_{D8}=10I_{D1} \), which gives an aspect ratio:

\[
\left( \frac{W}{L} \right) = 1046 \quad (10)
\]

Step 7: Compensating Capacitor \( C_C \):

For pole splitting additional capacitor is connected in feedback between the second and first stage which is calculated by

\[
GBW = \frac{2g_{mb1}}{2 \pi C_C} \quad (11)
\]
The Aspect ratio of all-transistor summarized in Table II.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Aspect Ratio(W/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>14.56µm/0.5µm(gm/Idrain)</td>
</tr>
<tr>
<td>Q2</td>
<td>14.6µm/1µm(gmb/Idrain)</td>
</tr>
<tr>
<td>Q3</td>
<td>14.6µm/1µm(gmb/Idrain)</td>
</tr>
<tr>
<td>Q4</td>
<td>14.6µm/1µm(gmb/Idrain)</td>
</tr>
<tr>
<td>Q5</td>
<td>14.6µm/1µm(gmb/Idrain)</td>
</tr>
<tr>
<td>Q6</td>
<td>14.56µm/0.5µm(gmb/Idrain)</td>
</tr>
<tr>
<td>Q7</td>
<td>29.7µm/1µm(gm/Idrain)</td>
</tr>
<tr>
<td>Q8</td>
<td>29.7µm/1µm(gm/Idrain)</td>
</tr>
<tr>
<td>Q9</td>
<td>29.7µm/1µm(gm/Idrain)</td>
</tr>
<tr>
<td>Q10</td>
<td>523µm/0.5µm(gm/Idrain)</td>
</tr>
</tbody>
</table>

Figure 6 shows the Frequency response with maximum gain 32.04dB and average power dissipation is 6.5nW.

III. VARIABLE GAIN AMPLIFIER

The Variable Gain Amplifier (VGA) is used for changing the gain of the amplifier according to the variation in the input signal. It is commonly used in an audio application where depends on signal amplitude, sound level is changed. There are many methods to gain-bandwidth the gain of an amplifier like feedback resistor, MRC, etc. as mentioned in the literature. In this paper, the method proposed in [11] applied where the gain control voltage is connected at the output stage. The control voltage at the gate changed the value of output impedance, hence gain is variable from a constant value. In this OTA, the gate of transistor Q11 connected with external control voltage to control the gain of the amplifier. For multiple values of control voltage, the gain and power dissipation are tabulated in Table III.

This is useful when the amplifier is used as a compressor in a hearing aid amplifier were for large input signals, less gain with small power dissipation is required.

<table>
<thead>
<tr>
<th>Control Voltage</th>
<th>Gain(dB)</th>
<th>Power Dissipation(nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.16V</td>
<td>21.9</td>
<td>6.11</td>
</tr>
<tr>
<td>0.18V</td>
<td>17.7</td>
<td>5.36</td>
</tr>
<tr>
<td>0.20V</td>
<td>10.72</td>
<td>4.74</td>
</tr>
<tr>
<td>0.22V</td>
<td>6.17</td>
<td>4.48</td>
</tr>
</tbody>
</table>

From Figure 7, it is possible to say that when the gain requirement is low the power dissipation low, and when the gain requirement is higher, the power dissipation is large. Hence, gain and power dissipation are directly related. So, for the variable gain amplifier is used to avoid unnecessary power dissipation by controlling the gain of the system. The Power Dissipation is low as compared to existing techniques with certain limitations. [2]-[10].

IV. CONCLUSION

In this paper Bulk driven Variable Gain OTA is designed and simulated for gain and power variation using gm/(gmb)/Idrain method for NMOS and PMOS. The results showed that with Vdd<Vth of 0.25V, the power dissipation in terms of Nano watt for the subthreshold operation of MOS devices. The graphical methods utilized for calculation of aspect ratio of MOS device. However, the proposed method has limitation of gain and gain-bandwidth product.

ACKNOWLEDGMENT

The author acknowledges the Visvesvaraya Ph.D. scheme for sponsoring the research work and publication.

REFERENCES
