A Low Voltage High Speed Segmented Current Steering DAC for Neural Stimulation Application

Jayeshkumar J. Patel, Amisha P. Naik

Abstract – A multi-phasic neural stimulator using current steering Digital to Analog Converter with low resolution is in great demand to ameliorate symptoms of Parkinson's disease and disorders of consciousness. This article presents 5-bit segmented DAC designed for such applications. In order to simulate the design, cadence virtuoso tool with 180 nm MOS technology is used. The results obtained after simulation indicate that the proposed DAC offers ±0.34 LSB INL and ±0.36 LSB value for DNL. For the input of 200 MSPS, the power dissipation is about 22 mW when working with 1.8 V of supply voltage.

Keywords-component; DAC, DNL, INL, Digital-to-analog converter, CMOS current-steering DAC, SFDR,

I. INTRODUCTION

DACs (Digital to Analog Converters) play a vital role in the various fields like biomedical instrumentation, Communication systems, Robotic, etc. Typically, the DACs are incorporated in most of the digital systems when the real-world signals. The real world signals like pressure signal, sound wave, temperature readings, or images are converted in digital form by means of analog-to-digital converters (ADCs). After processing, such signals are converted back to analog signals using DAC. DAC is an uncompromised requirement of the circuits those drive the devices ranging from audio – video applications, DC, AC or servo motor control to radio frequency transceivers or variety of industrial temperature controllers.

The common targets for stimulations of neural tissues lies within the central as well as at the peripheral nervous system (PNS). The CNS, central nervous system, is mainly concern with the proper functioning of neurons' population. The stimulation of the same is carried out for probing the said populations.

The stimulation also provides sensory feedback to its users utilizing the neuro prosthetic device. Clinically, to ameliorate symptoms of Parkinson's disease and epilepsy, the CNS stimulations are used. Similarly, for the sensory feedback of the prosthetic devices, the peripheral nervous system (PNS) stimulations are also useful [1,20]. In recent advancements, such simulation are applied to the treatment of hypertension and inflammatory disorders [2,20].

Modern VLSI technology enables miniaturized and fully implantable neuro stimulator circuits while simultaneously allowing the designer to integrate extremely large numbers of channels, and also allows increased functionality. Increased functionality empowers the designer to achieve higher stimulation efficacy without compromising the device size.

Revised Manuscript Received on January 15, 2020.

Prof. Jayeshkumar J. Patel, Research Scholar, Institute of Technology, Nirma University, Ahmedabad, India. E-mail:jayesh.patel@nirmauni.ac.in

Dr. Amisha P. Naik, Associate Professor, Institute of Technology, Nirma University, Ahmedabad, India. E-mail:amisha.naik@nirmauni.ac.in

Higher functionality helps to overcome the limitations encountered in the use of electrical stimulation such as non-specificity, which is reported in [20]. The modern VLSI technology can be applied to neuro stimulator systems for accurate simulations for the replacement of the traditional monopolar and bipolar counterpart [20].

The block diagram of a neural stimulator that utilizes multiple DACs in a single channel is shown in figure 1. DAC topology selection depends upon various parameters like chip area, amount of power require and accuracy of performance. Current steering DAC with Current source array of binary or unary weights and R – 2R ladders are part of famous topology that is utilized for the design of neuro stimulators.

The current steering DAC enables high power performance as the current sources transistors those involved in stimulation are required to be switched on. In case of a splitter, the entire circuit draws the current regardless of the selected node. However, in case of splitter the area increases linearly with increase in number of bits, which is not the case in the weighted arrays, where the area increases exponentially with the number of bits. Larger the number of bits in the weighted arrays higher the area required.

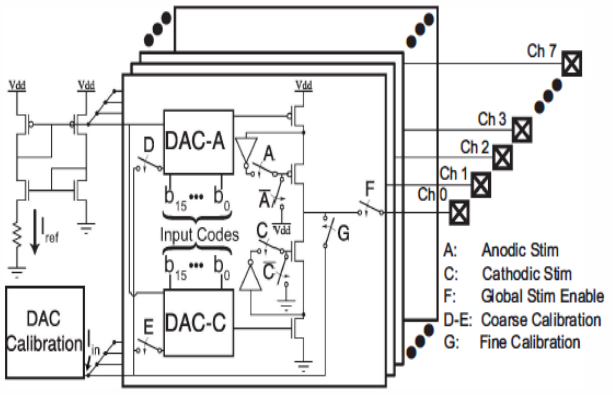

Fig.1: A block diagram of the neural stimulator for a single channel

II. CURRENT STEERING DAC

Current steering DACs are basically used for high frequency applications and for reduced consumption of power. This type of DAC must offer better performance in form of linearity error i.e. INL & DNL. Static performance mainly depends on the parameters like differential non-linearity (DNL), gain error, offset error and integral non-linearity (INL) while dynamic performance is affected by non-linearity such as glitches and time skew.

[1-3] reported that the high speed and low power consumption are vital issues in the design of data converters. General structure of N-bit DAC is represented as below in Fig-2.

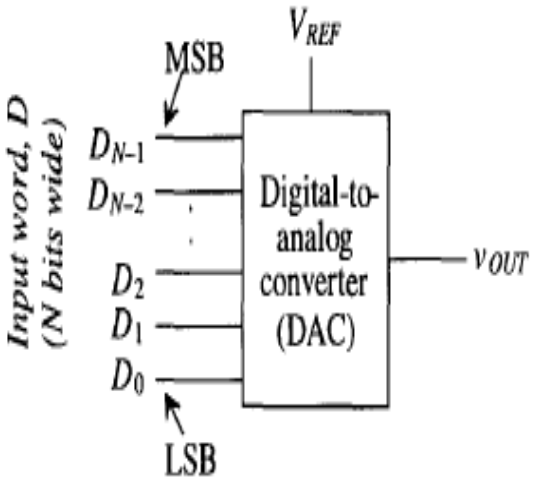

Fig.2: General representation of N-bit DAC

In DAC, a single continuous output value in the shape of current or voltage is generated through a set of binary levels. The signal which is continuous in amplitude and time domain is obtained from the signal which is discrete in both the said domains with the reference input voltage applied to the data converters. Current steering DAC among various types of DAC's are popular because of the fact that these data converters provide higher resolution with less consumption of power.

Digital-to-Analog Converter employing Current Steering topology has higher speed of conversion also supports increased resolution. To improve the matching precision of the current sources the Current Steering DAC is typically employed.

For N-bit DAC, output is expressed as follow:

$$V_{OUT} = \left(D_{N-1}\,2^{N-1} + \ldots + D_0\,2^0\right)\frac{V_{REF}}{2^N}$$

$$V_{OUT,\max} = \frac{2^{N-1}}{2^N}\cdot V_{REF}$$

Current Steering DACs are mainly classified in two ways namely Binary weighted and Unary weighted Current Steering DAC. In the former case, for N-bit DAC, N number of current sources are required. 4-bit binary weighted DAC is depicted as below shown in Fig-3:

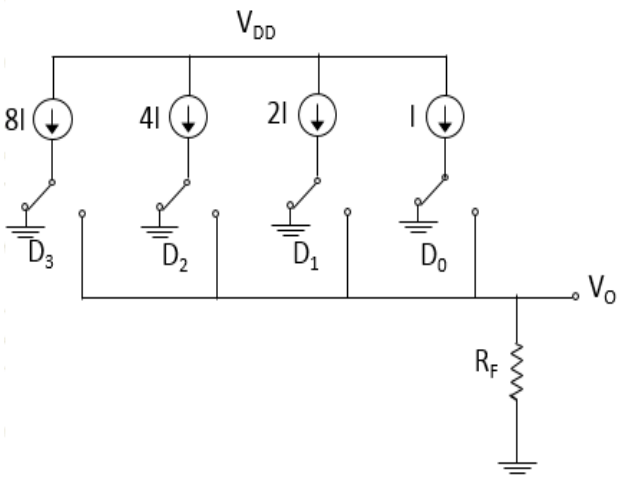

Fig.3: Current Steering DAC with 4 bit binary weight

In unary DAC, 2^N-1 current sources are required to convert N bit into analog signal. Each current source is having the same current value in this case. 3-bit unary weighted DAC is represented as shown in Fig-4.

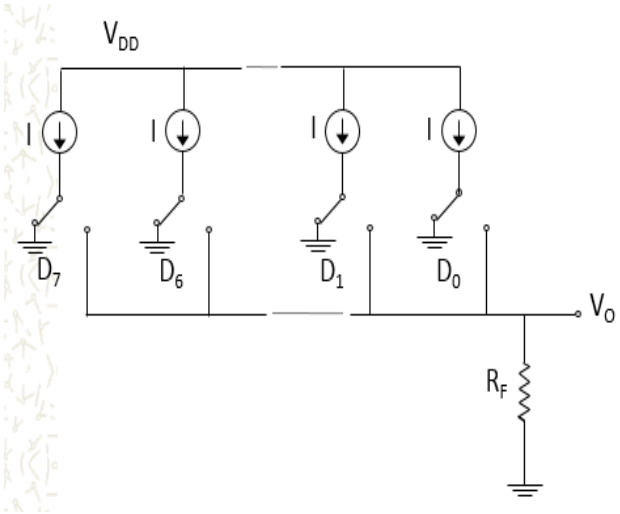

Fig.4: 3-bit current Steering DAC with unary weight

In binary weighted case, glitches are observed due to major transitions of bits, which results poor static performance in form of INL and DNL. While in case of unary weighted DAC, there will be no such chances but need more number of current sources which results more area.

A concept of segmented DAC can be used to trade off Static performance of DAC and area as well as power consumption.

The present work is focused to provide following merits over the existing designs reported in last decade. The design objective is to minimize DNL and INL without too much compromising power consumption and chip area for the application in Bio medical field. After carrying out thorough literature survey, simulations and analysis, following modifications are done to bring novelty in proposed DAC

For the proposed design and simulation, cadence tool is used with 180 nm CMOS technology. The proposed current steering DAC offers desired INL and DNL with rated power consumption.

III. SEGMENTED CURRENT STEERING DAC

A main source of nonlinearity originates because of glitches in the current cell. More no. of transitions results more no. of changes the states of switches say on to off or vice versa. In case of 5-bit binary weighted DAC, when input changes from 00111 to 01000, big glitch is observed because of 4 transitions. Similarly when input changes from 01111 to 10000, even big glitch will be there because of 5 transitions. In case of unary weighted DAC, there is only 1-bit transition so there is no glitch but it needs more no. of current sources; for 5 bit unary current steering DAC, 31 current sources of having same value are required. Thermometer code is used to control the switches. Additional hardware is required to convert binary code into thermometer codes. Binary to thermometer code conversion for 3 – bit is shown in Table - 1:

Table 1: Binary to thermometer code representation

Binary code	Thermometer code
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

To get the benefits of the both say binary weighted and unary weighted DAC, the concept of segmented DAC is explored. For DAC having N inputs, M bits have been implemented using unary weighted DAC while (N-M) bits to be implemented using binary weighted. The representation is as below shown in Fig-5 and Fig-6.

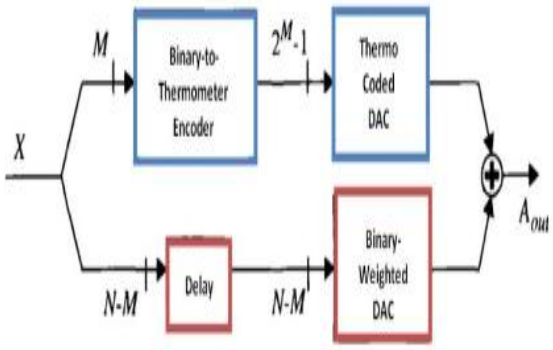

Fig. 5: Segmented DAC [3]

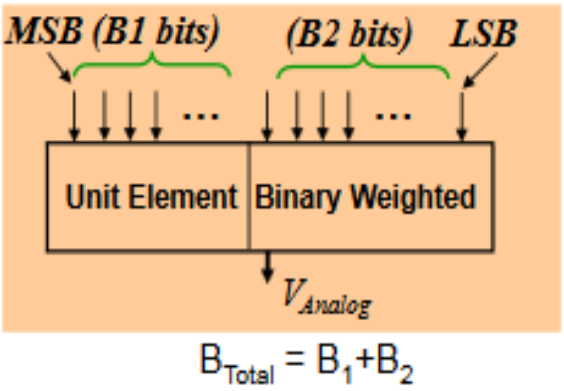

Fig. 6: Segmented DAC [3]

There are two approaches; in first approach, MSBs are implemented using unary weighted: for 5- bit DAC, if M=3, total no. of current sources are 7+2=9 (7 having same value of current ($4I_o$) while 2 are binary weighted say $2I_o$ & I_o), if M=2, total no. of current sources are 3+3=6 (3 having same value of current ($8I_o$) while 3 are binary weighted $4I_o$, $2I_o$ & I_o). In second approach, MSBs are implemented using Binary weighted: for 5- bit DAC, if M=3, total no. of current sources are 2+7=9 (7 having same value of current (I_o) while 2 are binary weighted say $16I_o$ & $8I_o$), if M=2, total no. of current sources are 3+3=6 (3 having same value of current (I_o) while 3 are binary weighted $16I_o$, $8I_o$ & $4I_o$).

Differential nonlinearity (acronym DNL) is a measure of error in DAC. It is defined as the deviation between two analog values corresponding to adjacent input digital values. DNL determines the accuracy of a DAC and can be given as:

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

Integral nonlinearity **(**acronym INL) is a commonly used measure of performance in DAC and ADC converters. In case of DACs, the deviation in the ideal output value compared to the actual measured output value for a certain input code is defined as INL.

IV. SIMULATION RESULTS AND DISCUSSIONS

The proposed 5-bit segmented current steering DAC is implemented in cadence virtuoso 180 nm technology. The DAC is simulated with supply voltage of 1.8 V and 200 MHz of the maximum sample rate. The simulated design consumes power of 20mW at sampling rate of 200 MHz. The simulated DNL and INL observed are ±0.36 LSB and ±0.34LSB, respectively.

Fig. 7 to Fig.12 shows the simulated results and output of proposed segmented DAC with compared to Binary weighted DAC.

Fig. 7 shows output in form of current for binary inputs. Major glitches are observed when input changes from 01111 to 10000.

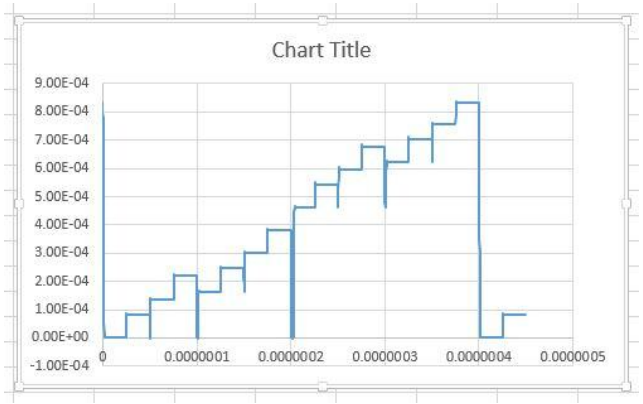

Fig.7: Output of binary weighted DAC

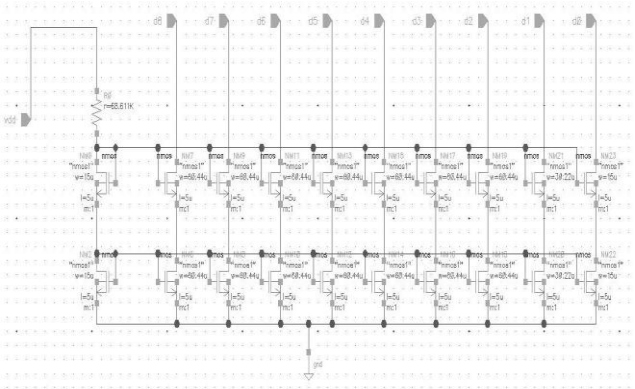

Fig.8: Architecture of segmented DAC

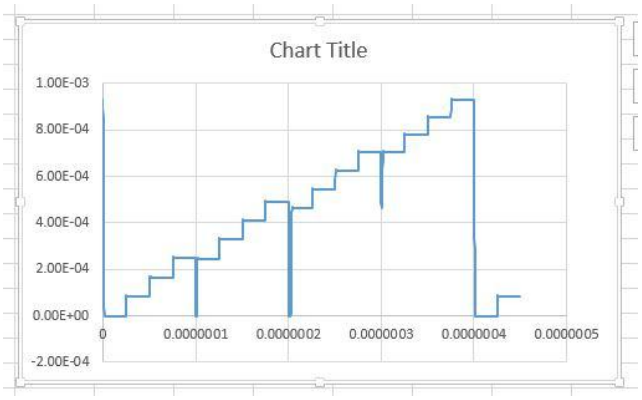

Fig.9: Current output of proposed DAC with lower weighted binary bits

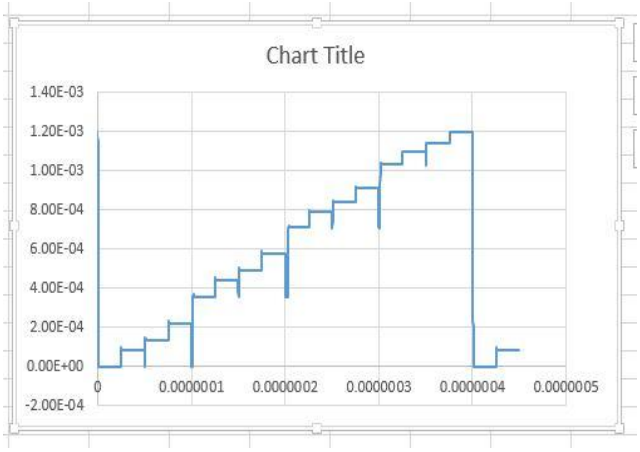

Fig.10: Current output of segmented DAC with lower weighted unary bits

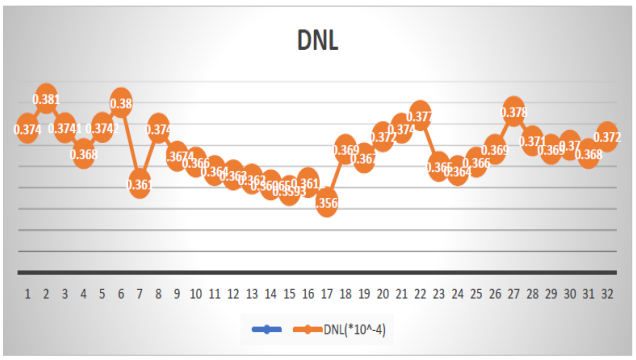

Fig.11: DNL graph of proposed segmented DAC

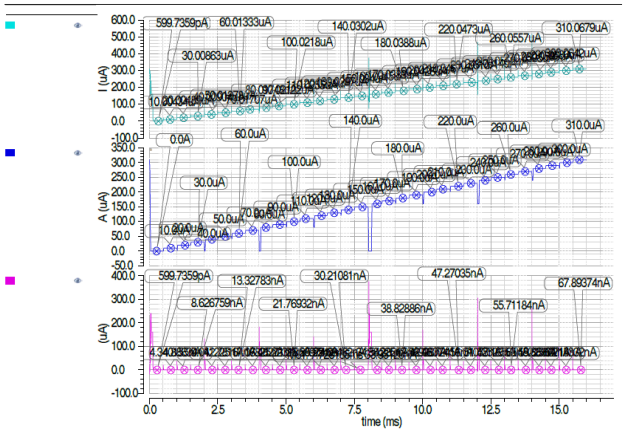

Fig.12: Plot of INL for proposed DAC

It has been observed that Glitches have been reduced in case of segmented DAC. Same is represented in Fig.9 and Fig.10.

The specifications of proposed DAC are as below:

Table 2: specifications of proposed DAC

Parameters	Proposed value
Technology	180
Resolution	5 bit
Approach	Segmented
Supply voltage	1.5-3.3 V
INL (Max)	0.34 LSB
DNL (Max)	0.36 LSB
Power (Max)	20mW
Frequency	200 Mhz

V. CONCLUSION

The novel architecture of current steering DAC for neural stimulation application is presented. It is observed that the Static error in the output current of the DAC mostly depends on type of switch, speed of switching and combination of segmentation. The proposed segmented DAC offers better static performance in form of INL and DNL. The result of DAC shows reduction in glitches which results in improvement in INL and DNL values. Total DC power dissipation is 22 mW at 1.8V. The proposed DAC offers a desirable performance in form of DNL and INL which is in the range of $\pm$0.5 LSB.

REFERENCES

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata Mac Graw Hill, 2005.
2. Baker, R. Jacob. CMOS: circuit design, layout, and simulation. Wiley-IEEE press, 2019.
3. Allen, Phillip E., and Douglas R. Holberg. CMOS analog circuit design. Elsevier, 2011.
4. Kim, Si-Nai, et al. "A SUC-Based Full-Binary 6-bit 3.1-GS/s 17.7-mW Current-Steering DAC in 0.038 mm^2." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.2 (2015): 794-798.
5. Taherzadeh-Sani, Mohammad, Reza Lotfi, and Frederic Nabki. "A 10-bit 110 kS/s 1.16µW SA-ADC With a Hybrid Differential/Single-Ended DAC in 180-nm CMOS for Multichannel Biomedical Applications." IEEE Transactions on Circuits and Systems II: Express Briefs 61.8 (2014): 584-588
6. Rahman, Md Tanvir, and Torsten Lehmann. "A self-calibrated cryogenic current cell for 4.2 K current steering D/A converters." IEEE Transactions on Circuits and Systems II: Express Briefs 64.10 (2016): 1152-1156.
7. Juanda, F. N. U., Wei Shu, and Joseph S. Chang. "A 10-GS/s 4-bit single-core digital-to-analog converter for cognitive ultrawidebands." IEEE Transactions on Circuits and Systems II: Express Briefs 64.1 (2016): 16-20.
8. Mukhopadhyay, Ishita, et al. "Dual-calibration technique for improving static linearity of thermometer DACs for I/O." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.3 (2015): 1050-1058.
9. Sarkar, Santanu, and Swapna Banerjee. "An 8-bit low power DAC with re-used distributed binary cells architecture for reconfigurable transmitters." Microelectronics Journal 45.6 (2014): 666-677.
10. Liu, Renzhi, and Larry Pileggi. "Low-overhead self-healing methodology for current matching in current-steering DAC." IEEE Transactions on Circuits and Systems II: Express Briefs 62.7 (2015): 651-655.

11. Pal, Neelanjana, et al. "Placement-based nonlinearity reduction technique for differential current-steering DAC." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.1 (2015): 233-242.
12. Park, Geunyeong, and Minkyu Song. "A CMOS current-steering D/A converter with full-swing output voltage and a quaternary driver." IEEE Transactions on Circuits and Systems II: Express Briefs 62.5 (2014): 441-445.
13. Li, Xueqing, et al. "A 14 bit 500 MS/s CMOS DAC using complementary switched current sources and time-relaxed interleaving DRRZ." IEEE Transactions on Circuits and Systems I: Regular Papers 61.8 (2014): 2337-2347.
14. Sarkar, Santanu, and Swapna Banerjee. "A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect." 2015 IEEE Computer Society Annual Symposium on VLSI. IEEE, 2015.
15. Przyborowski, Dominik, and Marek Idzik. "A 10-bit low-power small-area high-swing CMOS DAC." IEEE Transactions on Nuclear Science 57.1 (2010): 292-299.
16. Mohyar, Shaiful Nizam, and Haruo Kobayashi. "Digital calibration algorithm for half-unary current-steering DAC for linearity improvement." 2014 International SoC Design Conference (ISOCC). IEEE, 2014.
17. Mathurkar, Piyush, and Madan Mali. "Segmented 8-bit current-steering digital to analog converter." 2015 International Conference on Pervasive Computing (ICPC). IEEE, 2015.
18. Nag, Sudip, and Nitish V. Thakor. "Implantable neurotechnologies: electrical stimulation and applications." Medical & biological engineering & computing 54.1 (2016): 63-76.
19. Famm, Kristoffer, et al. "Drug discovery: a jump-start for electroceuticals." Nature 496.7444 (2013): 159.
20. Ng, Kian Ann, et al. "Implantable neurotechnologies: a review of integrated circuit neural amplifiers." Medical & biological engineering & computing 54.1 (2016): 45-62.

AUTHORS PROFILE

Prof. Jayeshkumar J. Patel
He is pursuing his Ph. D. From Nirma University, Ahmedabad in the field of mixed signal circuit design VLSI Design area. He has obtained his M. Tech from Institute of Technology, Nirma University, Ahmedabad in 2007 in the field of VLSI Design

He did his B.E from BVM Engineering College, Vallabh Vidyanagar. He has published many technical papers in national and international journals. He has more than 23 years of experience in teaching UG & PG students and industry

Dr. Amisha P. Naik, She is working as Associate professor at EC department, Nirma University, Ahmedabad since 2001. She teaches both at UG and PG level. She did B.E in Electronics from REC, Surat in the year 1997 and obtained M.Tech and Ph.D in VLSI Design area in the year 2006 and 2011 from Nirma University, Ahmedabad respectively. She has published many papers in national and international journals. She is guiding three ph. d students in the area of analog and mixed signal circuit design.